WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

a MOSFET formed on the substrate;

a first interconnection connected to a gate of the MOSFET;

a high concentration impurity diffused region located under the first interconnection and at a surface part of the semiconductor substrate;

a second interconnection connected to the high concentration impurity diffused region; and

a low resistance layer provided on the upper surface of the high concentration impurity diffused region.

2. The semiconductor device according to claim 1, wherein said high concentration impurity diffused region is enveloped by a device isolation film.

3. The semiconductor device according to claim 1, wherein said low resistance layer is a ~~metal~~ silicide layer.

4. The semiconductor device according to claim 1, wherein a potential same as that of the substrate or a well of the MOSFET is applied to the low resistance layer.

5. The semiconductor device according to claim 1, wherein said first interconnection constitutes a signal input pad for receiving an input signal for the MOSFET.

6. The semiconductor device according to claim 1, wherein a plurality of MOSFETs disposed in comb-like shape on the semiconductor substrate form an amplifier stage.

7. A semiconductor device comprising:

a semiconductor substrate;

a MOSFET formed ~~on~~ the substrate;

a first interconnection connected to a gate of the MOSFET;

a high concentration impurity diffused region located below the first interconnection and at a surface part of the semiconductor substrate;

a second interconnection connected to the high concentration impurity diffused region;

a low resistance layer provided on the upper surface of the high concentration impurity diffused region; and

a polysilicon layer provided below the first interconnection, said polysilicon layer being connected to the second interconnection.

8. The semiconductor device according to claim 7, wherein said high concentration impurity diffused region is enveloped by a device isolation film and wherein said polysilicon layer is provided on the device isolation layer.

9. The semiconductor device according to claim 8, wherein said low resistance layer is a metal silicide layer.

10. The semiconductor device according to claim 7, wherein the low resistance layer is also provided on the polysilicon layer.

11. The semiconductor device according to claim 7, wherein a potential same as that of the substrate or a well of the MOSFET is applied to the low resistance layer.

12. The semiconductor device according to claim 7, wherein said first interconnection constitutes a signal input pad for receiving an input signal for the MOSFET.

13. The semiconductor device according to claim 1, wherein a plurality of MOSFETs disposed in comb-like shape on the semiconductor substrate form an amplifier stage.

14. A method for manufacturing a semiconductor device comprising the steps of:

forming device isolation layer for defining a device region and a a high concentration impurity diffused region;

forming a gate electrode on a surface of the substrate within the device region;

implanting ions in the device region and the high concentration impurity diffused region with the device isolation layers and the gate electrode being as implantation mask;

depositing low resistance layer at least on the upper surface of the high concentration impurity diffused region;

depositing an inter-layer insulating film;

forming a first interconnection connected to the gate

electrode and a second interconnection connected to the high concentration impurity diffused region on the said inter-layer insulating film, at least the first interconnection being disposed so that it runs above the high concentration impurity diffused region.

15. The method according to claim 14, wherein said low resistance layer is ~~metal~~ a silicide layer deposited through a salicide process.

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